DEVICE REGISTER ADDRESSES:

Device	Registers		Address	Int Vector	Priority	NPR
CD11	Card Reader, high speed			230	BR4	X
	status & control	(CDST)	777 160			
	column count	(CDCC)	777 162			
	current address	(CDBA)	777 164			
	data	(CDDB)	777 166			
CR11	Card Reader			230	BR6	
	status	(CRS)	777 160			
	buffer, 12-bit char	(CRB1)	777 162			
	buffer, 8-bit char	(CRB2)	777 164			
KW11-L	Line Clock	(LKS)	777 546	100	BR6	
KW11-P	Programmable Clock			104	BR6	
	control & status		772 540			
	count set buffer		772 542			
	counter		772 544			
LA30,	Console Terminal					
LA36,	keyboard/reader status		777 560	60	BR4	
LT33,	keyboard/reader buffer		777 562			
VT05,	printer/punch status		777 564	64	BR4	
VT50	printer/punch buffer		777 566			
LP11,	Line Printer			200	BR4	
LS11,	printer status		777 514			
LV11	printer data		777 516			
PC11	Paper Tape					
	reader status	(PRS)	777 550	70	BR4	
	reader buffer	(PRB)	777 552			
	punch status	(PPS)	777 554	74	BR4	
	punch buffer	(PPB)	777 556			
RK11/	Disk Cartridge			220	BR5	X
RK05	drive status	(RKDS)	777 400			
	error	(RKER)	777 402			
	control & status	(RKCS)	777 404			
	word count	(RKWC)	777 406			
	current bus adrs	(RKBA)	777 410			
	disk address	(RKDA)	777 412			
	data buffer	(RKDB)	777 416			
RF11/	Disk			204	BR5	X
RS11	disk control status	(DCS)	777 460			
	word count	(WC)	777 462			
	current mem adrs	(CMA)	777 464			
	disk address	(DAR)	777 466			
	disk adrs ext & error	(DAE)	777 470			
	disk data buffer	(DBR)	777 472			
	maintenance	(MA)	777 474			
	adrs of disk segment	(ADS)	777 476			
RP11-C/	Disk			254	BR5	X
RP03,	device status	(RPDS)	776 710			
RPR11/	error	(RPER)	776 712			
RPR02	control status	(RPCS)	776 714			
	word count	(RPWC)	776 716			
	bus address	(RPBA)	776 720			
	cylinder address	(RPCA)	776 722			
	disk address	(RPDA)	776 724			
	maintenance 1	(RPM1)	776 726			
	maintenance 2	(RPM2)	776 730			
	maintenance 3	(RPM3)	776 732			
	selected unit cyl adrs	(SUCA)	776 734			
	silo memory	(SILO)	776 736			
RX11/	Floppy Disk			264	BR5	
RX01	command & status	(RXCS)	777 170			
	data buffer	(RXDB)	777 172			

Device	Registers		Address	Int Vector	Priority	NPR
RJP04/	Disk			254*	BR5**	X
RWP04/	control & status #1	(RPCS1)	776 700			
RP04	word count	(RPWC)	776 702			
	UNIBUS address	(RPBA)	776 704			
	desired sector/track address	(RPDA)	776 706			
	RH11 control & status	(RPCS2)	776 710			
	drive status	(RPDS)	776 712			
	error register #1	(RPER1)	776 714			
	attention summary	(RPAS)	776 716			
	look ahead	(RPLA)	776 720			
	data buffer	(RPDB)	776 722			
	maintenance register	(RPMR)	776 724			
	drive type	(RPDT)	776 726			
	serial number	(RPSN)	776 730			
	offset	(RPOF)	776 732			
	desired cylinder	(RPDC)	776 734			
	current cylinder	(RPCC)	776 736			
	error #2	(RPER2)	776 740			
	error #3	(RPER3)	776 740			
	ECC position	(RPEC1)	776 744			
	ECC pattern	(RPEC2)	776 746			
	bus address ext	(RPBAE)	776 750†			
	control & status #3	(RPCS3)	776 752†			
RJS04/	Disk			204*	BR5**	X
RWS04/	control & status #1	(RSCS1)	772 040			
RS04,	word count	(RSWC)	772 042			
RJS03/	UNIBUS address	(RSBA)	772 044			
RWS03	desired disk adrs	(RSDA)	772 046			
RS03	RH11 control & status	(RSCS2)	772 050			
	drive status	(RSDS)	772 052			
	error	(RSER)	772 054			
	attention summary	(RSAS)	772 056			
	look ahead	(RSLA)	772 060			
	data buffer	(RSDB)	772 062			
	maintenance	(RSMR)	772 064			
	drive type	(RSDT)	772 066			
	bus address ext	(RSBAE)	772 070†			
	control & status #3	(RSCS3)	772 072†			
TJU16/	Tape			224*	BR5**	X
TWU16/	control & status #1	(MTSC1)	772 440			
TU16	word count	(MTWC)	772 442			
	UNIBUS address	(MTBA)	772 444			
	frame count	(MTFC)	772 446			
	RH11 control & status	(MTCS2)	772 450			
	drive status	(MTDS)	772 452			
	error	(MTER)	772 454			
	attention summary	(MTAS)	772 456			
	check character	(MTCK)	772 460			
	data buffer	(MTDB)	772 462			
	maintenance	(MTMR)	772 464			
	drive type	(MTDT)	772 466			
	serial number	(MTSN)	772 470			
	tape control	(MTTC)	772 472			
	bus address ext	(MTBAE)	772 474†			
	control & status #3	(MTCS3)	772 476†			
TMA11/	Magnetic Tape			224	BR5	X
TU10,	status	(MTS)	772 520			
TS03	command	(MTC)	772 522			
	byte record cntr	(MTBRC)	772 524			
	current mem adrs	(MTCMA)	772 526			
	data buffer	(MTD)	772 530			
	read lines	(MTRD)	772 532			

*Jumper Selectable
**Plug Selectable
† Implemented on PDP-11/70 only

Device	Registers		Address	Int Vector	Priority	NPR
TA11	Cassette			260	BR6	
	command & status	(TACS)	777 500			
	data buffer	(TADB)	777 502			
TC11/	DECtape			214	BR6	X
TU56	control & status	(TCST)	777 340			
	command	(TCCM)	777 342			
	word count	(TCWC)	777 344			
	bus address	(TCBA)	777 346			
	data	(TCDT)	777 350			

BM873-YA BOOTSTRAP LOADER:

Starting Address	Device
773 000	RF11
773 010	RK11
773 020	Transfer to address contained in Switch Register
773 030	TC11
773 050	TM11
773 100	RP11
773 144	RC11
773 210	ASR paper tape reader
773 230	TA11
773 312	PC11

BM873-YB BOOTSTRAP LOADER:

Starting Address	Device	
773 000	RJS03/RJS04	Disk Unit 0
773 002	RJS03/RJS04	Unit specified in console switch register
773 030	RK11	Disk Unit 0
773 032	RK11	Unit specified in console switch register
773 070	TC11	
773 110	TM11	
773 136	RF11	
773 150	TJU16	
773 212	RC11	
773 320	RJP04	Disk Unit 0
773 322	RJP04	Unit specified in console switch register
773 344	Transfer to address in console switch register	
773 350	RP11	Disk Unit 0
773 352	RP11	Unit specified in console switch register
773 510	KL11/DL11	Console TTY Reader
773 524	TA11	Cassette Unit 0
773 526	TA11	Unit specified in console switch register
773 620	PC11	

PDP-11/70 BOOTSTRAP LOADER:

Starting Address 17 765 000

21 — 8	7 — 3	2 — 0
	DEVICE TYPE	UNIT #

Device Type:				
	1	TM11	6	TWU16
	2	TC11	7	RWP04
	3	RK11	10	RWS03/4
	4	RP11	11	RX11

ABSOLUTE LOADER

Starting Address: — 500
Memory Size:

4K	017
8K	037
12K	057
16K	077
20K	117
24K	137
28K	157
(or larger)	

BOOTSTRAP LOADER

Address	Contents	Address	Contents
— 744	016 701	— 764	000 002
— 746	000 026	— 766	— 400
— 750	012 702	— 770	005 267
— 752	000 352	— 772	177 756
— 754	005 211	— 774	000 765
— 756	105 711	— 776	177 560 (TTY) or 177 550 (PC11)
— 760	100 376		
— 762	116 162		

773 000 Paper Tape Bootstrap
773 100 Disk/DECtape Bootstrap
773 200 Card Reader Bootstrap
773 300 Cassette Bootstrap
773 400 Floppy Disk Bootstrap

MR11-DB BOOTSTRAP LOADER:

Starting Address	Device
773 100	RF11
773 110	RK11
773 120	TC11
773 136	TM11
773 154	RP11
773 220	RC11

7-BIT ASCII CODE:

Octal Code	Char	Octal Code	Char	Octal Code	Char	Octal Code	Char
000	NUL	040	SP	100	@	140	`
001	SOH	041	!	101	A	141	a
002	STX	042	"	102	B	142	b
003	ETX	043	#	103	C	143	c
004	EOT	044	$	104	D	144	d
005	ENQ	045	%	105	E	145	e
006	ACK	046	&	106	F	146	f
007	BEL	047	'	107	G	147	g
010	BS	050	(	110	H	150	h
011	HT	051	)	111	I	151	i
012	LF	052	*	112	J	152	j
013	VT	053	+	113	K	153	k
014	FF	054	,	114	L	154	l
015	CR	055	–	115	M	155	m
016	SO	056	.	116	N	156	n
017	SI	057	/	117	O	157	o
020	DLE	060	0	120	P	160	p
021	DC1	061	1	121	Q	161	q
022	DC2	062	2	122	R	162	r
023	DC3	063	3	123	S	163	s
024	DC4	064	4	124	T	164	t
025	NAK	065	5	125	U	165	u
026	SYN	066	6	126	V	166	v
027	ETB	067	7	127	W	167	w
030	CAN	070	8	130	X	170	x
031	EM	071	9	131	Y	171	y
032	SUB	072	:	132	Z	172	z
033	ESC	073	;	133	[	173	{
034	FS	074	<	134	\	174	|
035	GS	075	=	135	]	175	}
036	RS	076	>	136	^	176	~
037	US	077	?	137	—	177	DEL

digital pdp11

PROGRAMMING CARD

FOR FAMILY OF PDP-11 COMPUTERS

WORD FORMAT:

5	14 — 12	11 — 9	8 — 6	5 — 3	2 — 0	
						BINARY-OCTAL REPRESENTATION

MODE	R

Mode	Name	Symbolic	Description
0	register	R	(R) is operand [ex. R2=%2]
1	register deferred	(R)	(R) is address
2	auto-increment	(R)+	(R) is adrs; (R) + (1 or 2)
3	auto-incr deferred	@(R)+	(R) is adrs of adrs; (R) + 2
4	auto-decrement	–(R)	(R) – (1 or 2); (R) is adrs
5	auto-decr deferred	@–(R)	(R) – 2; (R) is adrs of adrs
6	index	X(R)	(R) + X is adrs
7	index deferred	@X(R)	(R) + X is adrs of adrs

PROGRAM COUNTER ADDRESSING: Reg = 7

MODE	7

2	immediate	#n	operand n follows instr
3	absolute	@#A	address A follows instr
6	relative	A	instr adrs + 4 + X is adrs
7	relative deferred	@A	instr adrs + 4 + X is adrs of adrs

LEGEND:

Op Codes

● = 0 for word/1 for byte
SS = source field (6 bits)
DD = destination field (6 bits)
R = gen register (3 bits), 0 to 7
XXX = offset (8 bits), +127 to –128
N = number (3 bits)
NN = number (6 bits)

Operations

( ) = contents of
s = contents of source
d = contents of destination
r = contents of register
← = becomes
X = relative address
% = register definition

Boolean

∧ = AND
V = inclusive OR
⊻ = exclusive OR
~ = NOT

Condition Codes

* = conditionally set/cleared
– = not affected
0 = cleared
1 = set

NOTE:

▲ = Applies to the 11/35, 11/40, 11/45 & 11/70 computers
● = Applies to the 11/45 & 11/70 computers

digital equipment corporation
MAYNARD, MASSACHUSETTS July 1975

pdp11

NUMERICAL OP CODE LIST:

OP Code	Mnemonic
00 00 00	HALT
00 00 01	WAIT
00 00 02	RTI
00 00 03	BPT
00 00 04	IOT
00 00 05	RESET
00 00 06	RTT
00 00 07 – 00 00 77	(unused)
00 01 DD	JMP
00 02 0R	RTS
00 02 10 ↕ 00 02 27	(unused)
00 02 3N	SPL
00 02 40	NOP
00 02 41 ↕ 00 02 77	cond codes
00 03 DD	SWAB
00 04 XXX	BR
00 10 XXX	BNE
00 14 XXX	BEQ
00 20 XXX	BGE
00 24 XXX	BLT
00 30 XXX	BGT
00 34 XXX	BLE
00 4R DD	JSR
00 50 DD	CLR
00 51 DD	COM
00 52 DD	INC
00 53 DD	DEC
00 54 DD	NEG
00 55 DD	ADC
00 56 DD	SBC
00 57 DD	TST

OP Code	Mnemonic
00 60 DD	ROR
00 61 DD	ROL
00 62 DD	ASR
00 63 DD	ASL
00 64 NN	MARK
00 65 SS	MFPI
00 66 DD	MTPI
00 67 DD	SXT
00 70 00 ↕ 00 77 77	(unused)
01 SS DD	MOV
02 SS DD	CMP
03 SS DD	BIT
04 SS DD	BIC
05 SS DD	BIS
06 SS DD	ADD
07 0R SS	MUL
07 1R SS	DIV
07 2R SS	ASH
07 3R SS	ASHC
07 4R DD	XOR
07 50 0R	FADD
07 50 1R	FSUB
07 50 2R	FMUL
07 50 3R	FDIV
07 50 40 ↕ 07 67 77	(unused)
07 7R NN	SOB
10 00 XXX	BPL
10 04 XXX	BMI
10 10 XXX	BHI
10 14 XXX	BLOS
10 20 XXX	BVC
10 24 XXX	BVS
10 30 XXX	BCC, BHIS
10 34 XXX	BCS, BLO

OP Code	Mnemonic
10 40 00 ↕ 10 43 77	EMT
10 44 00 ↕ 10 47 77	TRAP
10 50 DD	CLRB
10 51 DD	COMB
10 52 DD	INCB
10 53 DD	DECB
10 54 DD	NEGB
10 55 DD	ADCB
10 56 DD	SBCB
10 57 DD	TSTB
10 60 DD	RORB
10 61 DD	ROLB
10 62 DD	ASRB
10 63 DD	ASLB
10 64 00 ↕ 10 64 77	(unused)
10 65 SS	MFPD
10 66 DD	MTPD
10 67 00 ↕ 10 77 77	(unused)
11 SS DD	MOVB
12 SS DD	CMPB
13 SS DD	BITB
14 SS DD	BICB
15 SS DD	BISB
16 SS DD	SUB
17 00 00 ↕ 17 77 77	floating point

TRAP VECTORS:

000	(reserved)
004	Time Out & other errors
010	illegal & reserved instr
014	BPT instruction
020	IOT instruction
024	Power Fail
030	EMT instruction
034	TRAP instruction
114	Memory Parity
240	PIRQ, prog int req
244	Floating Point
250	Memory Management

SINGLE OPERAND: OPR dst

15 – 6	5 – 0
OP CODE	DD

Mnemonic	Op Code	Instruction	dst Result	N Z V C
General				
CLR(B)	■ 050DD	clear	0	0 1 0 0
COM(B)	■ 051DD	complement (1's)	~d	* * 0 1
INC(B)	■ 052DD	increment	d + 1	* * * –
DEC(B)	■ 053DD	decrement	d – 1	* * * –
NEG(B)	■ 054DD	negate (2's compl)	–d	* * * *
TST(B)	■ 057DD	test	d	* * 0 0
Rotate & Shift				
ROR(B)	■ 060DD	rotate right	→C, d	* * * *
ROL(B)	■ 061DD	rotate left	C, d←	* * * *
ASR(B)	■ 062DD	arith shift right	d/2	* * * *
ASL(B)	■ 063DD	arith shift left	2d	* * * *
SWAB	0003DD	swap bytes		* * * 0
Multiple Precision				
ADC(B)	■ 055DD	add carry	d + C	* * * *
SBC(B)	■ 056DD	subtract carry	d – C	* * * *
▲SXT	0067DD	sign extend	0 or –1	– * 0 –

DOUBLE OPERAND: OPR src, dst OPR src, R or OPR R, dst

15 – 12	11 – 6	5 – 0
OP CODE	SS	DD

15 – 9	8 – 6	5 – 0
OP CODE	R	SS OR DD

Mnemonic	Op Code	Instruction	Operation	N Z V C
General				
MOV(B)	■ 1SSDD	move	d ← s	* * 0 –
CMP(B)	■ 2SSDD	compare	s – d	* * * *
ADD	06SSDD	add	d ← s + d	* * * *
SUB	16SSDD	subtract	d ← d – s	* * * *
Logical				
BIT(B)	■ 3SSDD	bit test (AND)	s ∧ d	* * 0 –
BIC(B)	■ 4SSDD	bit clear	d ← (~s) ∧ d	* * 0 –
BIS(B)	■ 5SSDD	bit set (OR)	d ← s ∨ d	* * 0 –
▲Register				
MUL	070RSS	multiply	r ← r x s	* * 0 *
DIV	071RSS	divide	r ← r/s	* * * *
ASH	072RSS	shift arithmetically		* * * *
ASHC	073RSS	arith shift combined		* * * *
XOR	074RDD	exclusive OR	d ← r ⊻ d	* * 0 –

BRANCH: B – – location

If condition is satisfied:
Branch to location,
New PC ← Updated PC + (2 x offset)
$\underbrace{\text{Updated PC}}_{\text{adrs of br instr + 2}}$

15 – 8	7 – 0
BASE CODE	XXX

Op Code = Base Code + XXX

Mnemonic	Base Code	Instruction	Branch Condition	
Branches				
BR	000400	branch (unconditional)	(always)	
BNE	001000	br if not equal (to 0)	≠ 0	Z = 0
BEQ	001400	br if equal (to 0)	= 0	Z = 1
BPL	100000	branch if plus	+	N = 0
BMI	100400	branch if minus	–	N = 1
BVC	102000	br if overflow is clear		V = 0
BVS	102400	br if overflow is set		V = 1
BCC	103000	br if carry is clear		C = 0
BCS	103400	br if carry is set		C = 1
Signed Conditional Branches				
BGE	002000	br if greater or eq (to 0)	≥0	N ⊻ V = 0
BLT	002400	br if less than (0)	<0	N ⊻ V = 1
BGT	003000	br if greater than (0)	>0	Z v (N ⊻ V) = 0
BLE	003400	br if less or equal (to 0)	≤0	Z v (N ⊻ V) = 1
Unsigned Conditional Branches				
BHI	101000	branch if higher	>	C v Z = 0
BLOS	101400	branch if lower or same	≤	C v Z = 1
BHIS	103000	branch if higher or same	≥	C = 0
BLO	103400	branch if lower	<	C = 1

JUMP & SUBROUTINE:

Mnemonic	Op Code	Instruction	Notes
JMP	0001DD	jump	PC ← dst
JSR	004RDD	jump to subroutine	use same R
RTS	00020R	return from subroutine	use same R
▲MARK	0064NN	mark	aid in subr return
▲SOB	077RNN	subtract 1 & br (if ≠ 0)	(R) – 1, then if (R) ≠ 0: PC ← Updated PC – (2 x NN)

TRAP & INTERRUPT:

Mnemonic	Op Code	Instruction	Notes
EMT	104000 to 104377	emulator trap (not for general use)	PC at 30, PS at 32
TRAP	104400 to 104777	trap	PC at 34, PS at 36
BPT	000003	breakpoint trap	PC at 14, PS at 16
IOT	000004	input/output trap	PC at 20, PS at 22
RTI	000002	return from interrupt	
▲RTT	000006	return from interrupt	inhibit T bit trap

MISCELLANEOUS:

Mnemonic	Op Code	Instruction
HALT	000000	halt
WAIT	000001	wait for interrupt
RESET	000005	reset external bus
NOP	000240	(no operation)
●SPL	00023N	set priority level (to N)
▲MFPI	0065SS	move from previous instr space
▲MTPI	0066DD	move to previous instr space
●MFPD	1065SS	move from previous data space
●MTPD	1066DD	move to previous data space

CONDITION CODE OPERATORS:

15 – 5	4	3	2	1	0
OP CODE BASE = 000240		N	Z	V	C

Bit 4: 0 = CLEAR SELECTED COND CODE BITS; 1 = SET SELECTED COND CODE BITS

Mnemonic	Op Code	Instruction	N Z V C
CLC	000241	clear C	– – – 0
CLV	000242	clear V	– – 0 –
CLZ	000244	clear Z	– 0 – –
CLN	000250	clear N	0 – – –
CCC	000257	clear all cc bits	0 0 0 0
SEC	000261	set C	– – – 1
SEV	000262	set V	– – 1 –
SEZ	000264	set Z	– 1 – –
SEN	000270	set N	1 – – –
SCC	000277	set all cc bits	1 1 1 1

PROCESSOR REGISTER ADDRESSES:

Processor Status Word
PS - 777 776

15 – 14	13 – 12	11	10 – 8	7 – 5	4	3	2	1	0
CURRENT MODE ▲	PREVIOUS MODE ▲	GEN REG SET ●		PRIORITY	T	N	Z	V	C
					TRACE TRAP	NEGATIVE	ZERO	OVERFLOW	CARRY

00 = KERNEL ▲ 01 = SUPERVISOR ● 11 = USER ▲

▲Stack Limit Register — 777 774

●Program Interrupt Request — 777 772

General Registers (console use only)	R0 — 777 700	R4 — 777 704
	R1 — 777 701	R5 — 777 705
	R2 — 777 702	R6 — 777 706
(not for 11/45)	R3 — 777 703	R7 — 777 707

Console Switches & Display Register — 777 570

PDP-11/45, 11/70 FLOATING POINT PROCESSOR:

15 – 8	7 – 6	5 – 0
• OP CODE BASE = 170000	AC	SS OR DD

Mnemonic	Op Code	Instruction	Operation
CFCC	170000	copy fl cond codes	
SETF	170001	set floating mode	FD ← 0
SETI	170002	set integer mode	FL ← 0
SETD	170011	set fl dbl mode	FD ← 1
SETL	170012	set long integer mode	FL ← 1
LDFPS	1701 src	load FPP prog status	
STFPS	1702 dst	store FPP prog status	
STST	1703 dst	store (exc codes & adrs)	
CLRF, CLRD	1704 fdst	clear floating/double	fdst ← 0
TSTF, TSTD	1705 fdst	test fl/dbl	
ABSF, ABSD	1706 fdst	make absolute fl/dbl	fdst ← |fdst|
NEGF, NEGD	1707 fdst	negate fl/dbl	fdst ← –fdst
MULF, MULD	171 (AC) fsrc	multiply fl/dbl	AC ← AC x fsrc
MODF, MODD	171 (AC + 4) fsrc	multiply & integerize	
ADDF, ADDD	172 (AC) fsrc	add fl/dbl	AC ← AC + fsrc
LDF, LDD	172 (AC + 4) fsrc	load fl/dbl	AC ← fsrc
SUBF, SUBD	173 (AC) fsrc	subtract fl/dbl	AC ← AC — fsrc
CMPF, CMPD	173 (AC + 4) fsrc	compare fl/dbl (to AC)	
STF, STD	174 (AC) fdst	store fl/dbl	fdst ← AC
DIVF, DIVD	174 (AC + 4) fsrc	divide fl/dbl	AC ← AC/fsrc
STEXP	175 (AC) dst	store exponent	
STCFI, STCFL / STCDI, STCDL	175 (AC + 4) dst	store & convert fl or dbl to int or long int	
STCFD, STCDF	176 (AC) fdst	store & convert (dbl-fl)	
LDEXP	176 (AC + 4) src	load exponent	
LDCIF, LDCID / LDCLF, LDCLD	177 (AC) src	load & convert int or long int to fl or dbl	
LDCDF, LDCFD	177 (AC + 4) fsrc	load & convert (dbl-fl)	

PDP-11/35, 11/40 FLOATING POINT UNIT:

			N Z V C
FADD	07500R	floating add	* * 0 0
FSUB	07501R	floating subtract	* * 0 0
FMUL	07502R	floating multiply	* * 0 0
FDIV	07503R	floating divide	* * 0 0

POWERS OF 2:

n	2^n	n	2^n
0	1	10	1,024
1	2	11	2,048
2	4	12	4,096
3	8	13	8,192
4	16	14	16,384
5	32	15	32,768
6	64	16	65,536
7	128	17	131,072
8	256	18	262,144
9	512	19	524,288